Listing of Claims

The following listing of claims will replace all prior versions, and listings, of claims in the subject application:

1. (original) A layout design method for a semiconductor integrated circuit, comprising the steps of:

providing a cell layout library which stores structure information of functional cells and a plurality of groups of filler cells, each filler cell acting to fill space between the functional cells, one of the plurality of groups of filler cells containing an upper-layer metal and a lower-layer metal wherein the lower-layer metal has a power rail and a ground rail which are not connected to the upper-layer metal, and another of the plurality of groups of filler cells containing an upper-layer metal and a lower-layer metal wherein the lower-layer metal has a power rail and a ground rail one of which is connected to the upper-layer metal through a via;

arranging the functional cells on a layout based on the structural information from the layout library; and

arranging the filler cells of any of the plurality of groups selectively based on the structural information from the layout library so that the filler cells are arranged in channel regions where the functional cells are not located on the layout, each channel region being located at a predetermined distance from signal lines on the layout.

2. (original) The layout design method of claim 1 wherein the filler cells of at least one of the plurality of groups are arranged in the channel regions where standard cells and macro cells are not located on the layout, and power supply lines are arranged on the layout so that the filler cells of said at least one group are connected to the power supply lines.

3. (original) The layout design method of claim 1 wherein the filler cells of at least one of the plurality of groups which contain a bypass capacitor are arranged on the layout.

4. (original) The layout design method of claim 1 wherein the filler cells of at least two of the plurality of groups have a common configuration with respect to intermediate layers between an uppermost layer and a lowermost layer of the layout.

5. (original) The layout design method of claim 1 wherein the filler cells are selectively arranged in the channel regions on the layout so that metal layers of the filler cells which are not connected to the signal lines are connected to power supply lines on the layout.

6. (original) The layout design method of claim 1 wherein a duplicate arrangement of the filler cells of at least one of the plurality of groups is provided over a standard-cell region or a macro-cell region of the layout.

7. (original) A semiconductor integrated circuit which is created by a layout design method using a cell layout library which stores structure information of functional cells and a plurality of groups of filler cells, each filler cell acting to fill space between the functional cells, one of the plurality of groups of filler cells containing an upper-layer metal and a lower-layer metal wherein the lower-layer metal has a power rail and a ground rail which are not connected to the upper-layer metal, and another of the plurality of groups of filler cells containing an upper-layer metal and a lower-layer metal wherein the lower-layer metal has a power rail and a ground rail one of which is connected to the upper-layer metal through a via, the semiconductor

integrated circuit comprising:

the functional cells arranged on a layout based on the structural information from the layout library;

signal lines arranged on the layout; and

the filler cells of any of the plurality of groups selectively arranged based on the structural information from the layout library so that the filler cells are arranged in channel regions where the functional cells are not located on the layout, each channel region being located at a predetermined distance from the signal lines on the layout.

8. (original). The semiconductor integrated circuit of claim 7 wherein the filler cells of at least one of the plurality of groups are arranged in the channel regions where standard cells and macro cells are not located on the layout, and power supply lines are arranged on the layout so that the filler cells of said at least one group are connected to the power supply lines.

9. (original) The semiconductor integrated circuit of claim 7 wherein the filler cells of at least one of the plurality of groups which contain a bypass capacitor are arranged on the layout.

10. (original) The semiconductor integrated circuit of claim 7 wherein the filler cells of at least two of the plurality of groups have a common configuration with respect to intermediate layers between an uppermost layer and a lowermost layer of the layout.

11. (original) The semiconductor integrated circuit of claim 7 wherein the filler cells are selectively arranged in the channel regions on the layout so that metal layers of the filler cells which are not connected to the signal lines are connected to power supply lines on the layout.

12. (original) The semiconductor integrated circuit of claim 7 wherein a duplicate arrangement of the filler cells of at least one of the plurality of groups is provided over a standard-cell region or a macro-cell region of the layout. .

13. (new) The layout design method of claim 1 wherein the arrangement of the filler cells in the channel regions connects power supply wiring of the upper layer metal and power supply wiring of the lower-layer metal.

14. (new) The layout design method of claim 13 wherein the arrangement of the filler cells in the channel regions connects said upper layer metal to one of said power rail and said ground rail of said lower-layer metal.

15. (new) The layout design method of claim 1 wherein the filler cells are arranged in the channel regions after wiring of signal lines is performed.